CLAIMS

What is claimed is:

1. An optical transfer system for converting an externally-applied video signal into an optical signal and for restoring the optical signal to the original video signal, the system comprising:

a video controller for separating color signals and a horizontal/vertical synchronous signal from an original video signal, and for transmitting the color signals and the horizontal/vertical synchronous signal in response to externally-applied predetermined data enable signal and clock signal;

a transmitter for skew-compensating and compressing signals received from the video controller and for converting the compressed signals to a driving current;

a transmission photo diode for converting the driving current to an optical signal and for outputting the optical signal;

an optical transmission line comprised of a predetermined number of channels, for transmitting the optical signal;

a reception photo diode for converting the optical signal received from the optical transmission line into a current signal and for outputting the current signal; and

a receiver for converting the current signal into a voltage signal, for decompressing the voltage signal, for compensating for the skew of the voltage signal, and for restoring the original signal.

2. The optical transfer system of claim 1, wherein the transmitter comprises:

a phase locked loop for generating a clock signal synchronized with an externally-generated clock signal, and for outputting the synchronized clock signal to serve as a clock signal for data transmission;

a skew compensator for receiving data, each data having a predetermined number of bits, from the video controller, in response to the synchronized clock signal,

via different channels, and compensating for a skew which is generated between the channel data in response to the synchronized clock signal;

a scrambler for counting the number of high levels and the number of low levels of each of the skew-compensated channel data, and adding the counted information to each of the channel data to serve as direct current balance information, and transmitting the resultant data;

a data serialization unit for compressing the scrambled channel data in response to the synchronized clock signal to obtain 1-bit channel data; and

an optical driver for receiving the compressed channel data and the clock signal as different channel data and converting the received data into current signals, in order to drive the transmission photo diode.

3. The optical transfer system of claim 2, wherein the optical driver comprises:

a bias and modulation resistance variation unit including a bias resistor and a modulation resistor, the resistance value of each of which is variable, for varying a current amount, which is output due to variations in the resistance values of the bias resistor and the modulation resistor;

a bandgap circuit for determining a bandgap reference voltage, which is maintained to a constant value independently of external changes, and for varying a bias current or a modulation current according to the determined reference voltage and current variations due to variations in the resistance of the bias resistor and the modulation resistor; and

a laser driver for converting received channel data into current signals and for adding the modulation current and bias current of the current signals to obtain a driving current for driving external optical devices.

4. The optical transfer system of claim 3, wherein the bandgap circuit comprises:

a bandgap reference voltage generator for compensating according to a variation in the voltage of a first node, which is a basis for voltage determination, so that the voltage of the first node maintained at a constant value, and for operationally amplifying the bandgap reference voltage and a voltage at the modulation resistor while operationally amplifying the bandgap reference voltage and a voltage at the bias resistor, thereby to obtain first and second output voltages, respectively;

a bias and modulation current generator for constantly maintaining the first and second output voltages and the voltages at the modulation resistor and the bias resistor by feeding the first and second output voltages back to the bandgap reference voltage generator, and for varying the modulation or bias current in response to the voltages at the modulation resistor or the bias resistor; and

a power save controller having at least one switch, which is switched in response to an externally-input power save control signal, for converting the modes of the bandgap reference voltage generator and the bias and modulation current generator into sleep modes in response to the switching of the switches.

5. The optical transfer system of claim 3, wherein the laser driver comprises:

a data separation unit for splitting the channel data into a non-inverted signal and an inverted signal to obtain a non-inverted output signal and an inverted output signal; and

a voltage-to-current conversion and current driving unit for calculating the voltage difference between the non-inverted output signal and the inverted output signal to obtain a current corresponding to the voltage difference, and for adding the current to the bias current and the modulation current to obtain the driving current.

6. The optical transfer system of claim 1, wherein the receiver comprises:

an optical receiver for converting current signals received from the reception photo diode into voltage signals, and for duty-compensating and level-converting the voltage signals to obtain digitalized signals which are different channel data; and

a phase locked loop for generating a clock signal which synchronizes with a clock signal included in the channel data, and for outputting the synchronized clock signal to serve as an actual clock signal for data reception;

a data restoration and skew compensation unit for receiving channel data that has been compressed by the transmitter, for decompressing the compressed data in response to the synchronized clock signal, and for skew-compensating the decompressed data to obtain different channel data each having a predetermined number of bits; and

a descrambler for descrambling in response to the direct current balance information in each of the channel data, so that the low level and high level of the channel data balance with each other.

7. The optical transfer system of claim 6, wherein the optical receiver comprises:

a bias circuit for receiving a predetermined amount of current from a power supply voltage and generating first and second bias currents;

a current-to-voltage converter for sourcing a current in response to the first bias current and converting a current signal received from the reception photo diode into a differential voltage signal;

an amplifier for sourcing a current in response to the first bias current and amplifying the differential voltage signal to obtain first and second differential output signals;

a duty compensator realized with different comparators having a current summing structure in which output currents are summed, the duty compensator for sourcing a current in response to the first bias current and comparing the first

differential output signal with a first reference voltage and the second differential output signal with a second reference voltage to obtain first and second output signals which correspond to the compared results;

a level converter for sourcing a current in response to the second bias current and digitalizing the first and second output signals by converting the voltage levels of the first and second output signals; and

a buffer unit for buffing and amplifying signals received from the level converter to obtain the digital channel data.

8. The optical transfer system of claim 6, wherein the optical receiver further comprises a power down controller for powering down the bias circuit so that it does not operate, in response to an externally-applied power down control signal.

9. The optical transfer system of claim 6, wherein the data restoration and skew compensation unit comprises:

a first latch unit for latching data received in series from the optical receiver, in units of n+N−1 (where N is a positive integer greater than or equal to 3) bits in parallel in response to first through n-th non-overlapped clock signals, and outputting N n-bit latched state data having the time difference of a predetermined offset therebetween;

a second latch unit for latching in parallel the N state data in response to an X-th ($1 \leq X \leq n$) non-overlapped clock signal having the greatest timing margin among the first through n-th non-overlapped clock signals; and

a synchronizer for outputting state data from which the synchronous signal is detected, among data latched by the second latch unit, as restored information data, in response to a predetermined synchronous existence signal and the X-th non-overlapped clock signal,

wherein the first through n-th non-overlapped clock signals are generated by the phase locked loop, and each has a predetermined offset so that the clock signals are not overlapped with each other.

10. An optical driver in a transmitter for transmitting externally-input channel data via an optical transmission line, as an optical signal, the optical driver comprising:

a bias and modulation resistance variation unit including a bias resistor and a modulation resistor, the resistance value of each of which is variable, for varying a current amount which is output due to variations in the resistance values of the bias resistor and the modulation resistor;

a bandgap circuit for determining a bandgap reference voltage, which is always maintained to a constant value independently of external changes, and varying a bias current or a modulation current according to the determined reference voltage and current variations due to variations in the resistance of the bias resistor and the modulation resistor; and

a laser driver for converting received channel data into current signals and adding the modulation current and bias current of the current signals to obtain a driving current for driving external optical devices.

11. The optical driver of claim 10, wherein the bandgap circuit comprises:

a bandgap reference voltage generator for compensating according to a variation in the voltage of a first node which is a basis for voltage determination, so that the voltage of the first node is constantly maintained, and operationally amplifying between the bandgap reference voltage and a voltage at the modulation resistor and between the bandgap reference voltage and a voltage at the bias resistor to obtain first and second output voltages, respectively;

a bias and modulation current generator for constantly maintaining the first and second output voltages and the voltages at the modulation resistor and the bias

resistor by feeding the first and second output voltages back to the bandgap reference voltage generator, and varying the modulation or bias current in response to the voltages at the modulation resistor or the bias resistor; and

a power save controller having at least one switch, which is switched in response to an externally-input power save control signal, the switch for converting the modes of the bandgap reference voltage generator and the bias and modulation current generator into sleep modes in response to the switching of the switches.

12. The optical driver of claim 10, wherein the laser driver comprises:

a data separation unit for splitting the channel data into a non-inverted signal and an inverted signal to obtain a non-inverted output signal and an inverted output signal; and

a voltage-to-current conversion and current driving unit for calculating the voltage difference between the non-inverted output signal and the inverted output signal to obtain a current corresponding to the voltage difference, and adding the current to the bias current and the modulation current to obtain the driving current.

13. The optical driver of claim 10, wherein the data separation unit obtains the non-inverted output signal and the inverted output signal having the same delay time.

14. An optical receiver in a receiver for receiving channel data which is converted into a current signal by an external photo diode, the optical receiver comprising:

a bias circuit for receiving a predetermined amount of current from a power supply voltage and generating first and second bias currents;

a current-to-voltage converter for sourcing a current in response to the first bias current and converting a current signal received from the reception photo diode into a differential voltage signal;

an amplifier for sourcing a current in response to the first bias current and amplifying the differential voltage signal to obtain first and second differential output signals;

a duty compensator realized with different comparators having a current summing structure in which output currents are summed, the duty compensator for sourcing a current in response to the first bias current and comparing the first differential output signal with a first reference voltage and the second differential output signal with a second reference voltage to obtain first and second output signals which correspond to the compared results; and

a level converter for sourcing a current in response to the second bias current and digitalizing the first and second output signals by converting the voltage levels of the first and second output signals.

15. The optical receiver of claim 14, further comprising a buffer unit for buffing and amplifying signals received from the level converter to obtain the channel data.

16. The optical receiver of claim 14, wherein the optical receiver further comprises a power down controller for powering down the bias circuit so that it does not operate, in response to an externally-applied power down control signal.

17. The optical receiver of claim 14, wherein the duty compensator differentiates the first and second differential output signals and sets the resultant signals to be first and second reference voltages, respectively.

18. The optical receiver of claim 15, wherein the buffer unit includes a plurality of inverters which are connected to each other in series, and each of a plurality of transistors constituting the inverters is larger than the previous transistor by a multiple of 2K (where K is a natural number greater than or equal to 0).

19. A data restoration and skew compensation unit in a receiver having a phase locked loop for generating first through n-th non-overlapped clock signals, each having a predetermined offset to prevent mutual overlapping, the receiver for restoring data in which n-bit synchronous signals (where n is a positive integer greater than or equal to 1) and n-bit information data are multiplexed and transmitted in series via a transmission channel, in response to the first through n-th non-overlapped clock signals, the data restoration and skew compensation unit comprising:

a first latch unit for latching received serial data in units of n+N−1 (where N is a positive integer greater than or equal to 3) bits in parallel in response to the first through n-th non-overlapped clock signals, and for outputting N n-bit latched state data having the time difference of a predetermined offset therebetween;

a second latch unit for latching in parallel the N state data in response to an X-th ($1 \leq X \leq n$) non-overlapped clock signal having the greatest timing margin among the first through n-th non-overlapped clock signals; and

a synchronizer for outputting state data from which the synchronous signal is detected, among data latched by the second latch unit, as restored information data, in response to a predetermined synchronous existence signal and the X-th non-overlapped clock signal.

20. The data restoration and skew compensation unit of claim 19, wherein the predetermined offset is the width of a unit bit constituting the serial data.

21. The data restoration and skew compensation unit of claim 19, wherein the first latch unit comprises:

first through (n+N−1)th flip flops for data-receiving bit units constituting the received serial data, and for clock-receiving the first through n-th non-overlapped clock signals; and

first through N-th buffers for buffering the data output of **n** flip flops among the first through (n+N−1)th flip flops and outputting the buffered results as the state data.

22. The data restoration and skew compensation unit of claim 19, wherein the synchronizer comprises:

a selector for selectively outputting the N state data in response to a selection signal;

a state and selection signal generator for comparing state data selected by the selector with the bit pattern of the synchronous signal in response to the sync existence signal and a current state signal representing the current state, and for outputting the selection signal and a next state signal representing the next state, in response to the results of the comparison; and

an (N+1)th buffer for buffering the next state signal in response to the X-th non-overlapped clock signal and outputting the result of buffering as the current state signal,

wherein the restored information data is state data selected by the selector when the state data is consistent with the bit pattern of the synchronous signal.

23. A method of restoring information data from data in which n-bit synchronous signals (where n is a positive integer greater than or equal to 1) and the n-bit information data are multiplexed and transmitted together with a clock signal in series via a transmission channel, the method comprising:

(a) generating first through n-th non-overlapped clock signals, each having a predetermined offset to prevent mutual overlapping, on the basis of the clock signal;

(b) latching received serial data in units of n+N−1 (where N is a positive integer greater than or equal to 3) bits in parallel in response to the first through n-th non-overlapped clock signals;

(c) generating ~~N-bit~~ N n-bit latched state data having the time difference of a predetermined offset therebetween;

(d) latching in parallel the N state data in synchronization with a X-th ($1 \leq X \leq n$) non-overlapped clock signal having the greatest timing margin among the first through n-th non-overlapped clock signals; and

(e) determining state data from which the synchronous signal is detected, among the latched state data, to be the restored information data, when the serial data is the synchronous signal.

24. The method of claim 23, wherein the step (e) comprises:

(e1) determining whether the first state data, which synchronizes with the clock signal, among the state data, is consistent with the bit pattern of the synchronous signal, when the serial data is the synchronous signal;

(e2) determining the first state data to be the restored information data, when the first state data is equal to the bit pattern;

(e3) determining whether the second state data, which is lagged by the predetermined offset with respect to the first state data, among the state data, is consistent with the bit pattern of the synchronous signal, if the first state data is not consistent with the bit pattern of the synchronous signal;

(e4) determining the second state data to be the restored information data, when the second state data is equal to the bit pattern;

(e5) determining whether the third state data, which leads by the predetermined offset with respect to the first state data, among the state data, is consistent with the bit

pattern of the synchronous signal, if the second state data is not consistent with the bit pattern of the synchronous signal;

(e6) determining the third state data to be the restored information data, when the third state data is equal to the bit pattern; and

(e7) feeding back to the step (e1) if the third state data is not consistent with the bit pattern of the synchronous signal,

wherein after the first, second or third state data is determined to be the restored information data, if it is not consistent with the bit pattern, the step (e1) is preformed.